CONTINUOUS INTERNAL EVALUATION– 2

Dept:CSE	Sem / Div: 3/A&B	Sub:Computer Organization	S Code:18CS34
Date:02/12/2020	Time: 2:30-4:00	Max Marks: 50	Elective:N
Note: Answer any 2 full questions, choosing one full question from each part.			

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QN		Questions	Marks	RBT	COs
		PART A			
1	a	Draw and explain the internal organization of 2M*8 asynchronous DRAM chip.	10	L2	CO2
	b	Define ROM and explain various types of ROMs.	10	L2	CO2
	c	Calculate the average access time experienced by a processor, if miss penalty is 17 clock cycles and miss rate is 10% and cache access time is 1 clock cycle.	5	L3	CO2
		OR			
2	a	Describe different types of cache mapping techniques with diagram.	10	L2	CO2
	b	Describe the organization of an 2M x 32 memory using 512K x 8 static memory chips	10	L2	CO2
	c	Consider a cache consisting of 256 blocks of 16 words each, for a total of 4096 words and assume main memory is addressable by 16 bit address and consists of 4K blocks. How many bits are there in each of Tag, block/set and word fields for different mapping techniques[Consider 2 block sets for set associative mapping]	5	L3	CO2
		PART B			
3	a	Design the 16 bit carry look ahead adder using 4-bit adders.	10	L2	CO4
	b	Perform the operations on 5 bit signed numbers using 2's complement system. Also indicate whether overflow has occurred. i) (-10) + (-13) ii) (-10)-(-13) iii)(-2)+(-9) iv)(-14)+ (+11) v)(-5)-(-7)	10	L3	CO4
	c	Write a note on memory hierarchy with respect to speed, size and cost.	5	L2	CO2
		OR			
4	a	Explain the logic diagram of 4 bit carry look ahead adder and its operations.	10	L2	CO4
	b	Perform the operations on 4 bit signed numbers using 2's complement system. Also indicate whether overflow has occurred. i) (+4) + (-6) ii) (-3)-(-7) iii)(4)+(3) iv)(+2)-(-3) v)(+6)-(+3)	10	L3	CO4
	c	Explain the structure of Synchronous DRAM	5	L2	CO2